AN10418

Level shifting I²C-bus buffers

Rev. 1 — 11 November 2010 Application note

Document information

Info	Content
Keywords	I2C, level shifting, bus buffer
Abstract	NXP Semiconductors family of level shifting bus buffers are detailed in this application note that discusses device operation, maximum cable length and frequency calculations and typical applications.

Revision history

Rev	Date	Description
v.1	20101111	application note; initial version

Contact information

For more information, please visit: **http://www.nxp.com**

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1. Introduction

1.1 Description

PCA9507/08/09/12A/17A/19/27 series of level shifting I²C-bus buffers with two dedicated supply voltage pins provides level shifting between low voltage (down to 0.9 V) and higher voltage (2.7 V to 5.5 V) for I²C-bus or SMBus applications. While retaining all the operating modes and features of the I²C-bus system during the level shifts, it also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enables the system designer to isolate two halves of a bus for both voltage and capacitance, and perform hot-swap and voltage level translation. Furthermore, the dual supply pins can be powered up in any sequence; when any of the supply pins are unpowered, the 5 V tolerant I/O are high-impedance.

PCA9507/08/09/12A/17A/19/27 allow a larger or longer I²C-bus or SMBus system where the following constraints previously restricted its size:

- More I²C-bus devices or larger wiring capacitance than the 400 pF maximum allowed in the I²C-bus specifications
- Long bus wiring or multipoint backplane traces
- Different operating supply voltages or logic voltage levels within one system
- Isolation of a section of a system that has lost its power supply
- Insertion of unpowered cards into an active I²C-bus

The PCA9507/08/09/12A/17A/19/27 are designed to work with I²C clock frequencies up to 400 kHz and are suitable for utilization in a multi-master I²C-bus or SMBus environment. They are specifically designed for backplane multipoint applications and level shifting applications. The devices support bus arbitration and contention with bus masters located on any segment. They are bidirectional and require no direction control.

Operational voltage supply is 2.7 V to 5.5 V with 5.5 V tolerant I/Os.

Operational temperature range is −40 °C to +85 °C.

1.2 Applications

These level shifting devices can be used for a wide variety of applications:

- I²C-bus or SMBus extension
- I²C-bus or SMBus isolation
- Voltage translation
- Level shifting slave cards
- Internal current source as pull-up resistor substitution

1.2.1 I²C-bus or SMBus extension

The PCA9507/08/09/12A/17A/19/27 level shifting bus buffers support two I²C-bus or SMBus branches of 400 pF as shown in Figure 1. They allow extension of the I²C-bus or SMBus on systems requiring capacitance loads larger than the 400 pF (max.) specified by the I²C-bus protocol. Designers can extend the use of the I²C-bus or SMBus in systems with more devices and/or longer bus lengths with only one repeater delay between any devices. The devices are multi-master capable and support arbitration and bus contention on any segment.

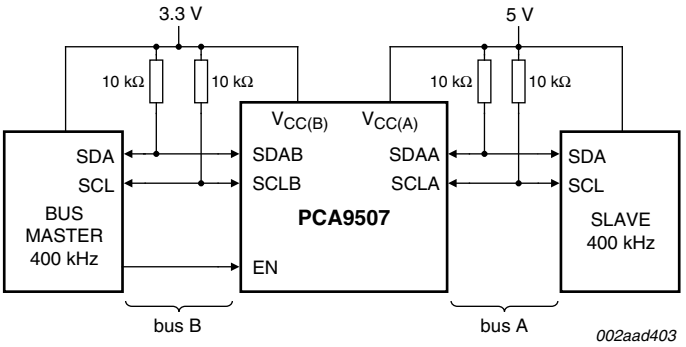


Fig 1. Typical level shifting bus buffer application

1.2.2 I²C-bus or SMBus isolation

The PCA9507/08/09/12A/17A/19/27 have an individual repeater channel with an enable/disable feature that can be used to electrically isolate that segment of the I²C-bus or SMBus. All devices release their I/O pins should their supply voltage fail.

Examples where this isolation feature could be useful include:

- Allow mixed operation of 100 kHz and 400 kHz devices on a combined bus by isolating the segment with 100 kHz devices from the rest of the 400 kHz system so that the 400 kHz devices can operate at their maximum speed.
- Supporting the PCI management bus with 8 or more PCI slots.
- Sensing multiple power supplies on different bus segments and providing automatic isolation of failed segments or segments suffering ‘brownout’ of their power supplies.

1.2.3 Level shifting or voltage translation

The PCA9507/08/09/12A/17A/19/27 also support logic level translations since either side voltage can range from 2.7 V to 5.5 V and both sides do not need to be at the same voltage level.

The GTL2000/02/03/10, PCA9306 and NVT family of non-buffering devices allow I²C voltage level translation at any voltage between 1.0 V and 5.0 V to any voltage between 1.0 V and 5.0 V. See application note *AN10145, “Bidirectional low voltage translators”* for more information on the use of these passive devices to support voltage level translations. These GTL-TVC devices are less expensive than the PCA9507/08/09/12A/17A/19/27 level shifting bus buffers, but do not isolate the bus capacitance and rise time is dependant on the RC time constant.

1.2.4 Internal current source as pull-up resistor substitution

The PCA9509/19 has a 1 mA internal current source. This current source is substituted for the external bus pull-up resistors normally found on the backplane I²C-bus. If each card uses the PCA9509/19, as cards are added or removed, the I²C-bus RC time constant stays the same, since as card capacitance is added the effective resistance decreases.

1.3 Device features and characteristics

- Bidirectional buffer for the SDA and SCL lines designed to prevent I²C-bus corruption during live board insertion and removal from the backplane using enable feature
- Compatible with I²C-bus Standard-mode, I²C-bus Fast-mode, and SMBus standards; multi-master capable
- $\Delta V/\Delta t$ rise time accelerators SDA and SCL lines
- Low I_{CC} chip enable/disable: < 1 mA
- Wide operating voltage range with 5.5 V tolerant I²C and ENABLE pins
- Two V_{CC} pins for optimal level shifting
- Operating temperature range is −40 °C to +85 °C
- Accommodate 100 kHz and 400 kHz devices and multiple masters
- ESD protection exceeds:
  - 2000 V HBM per JESD22-A114
  - 200 V MM per JESD22-A115
  - 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Offered in 8-pin SO (D) and TSSOP (MSOP) (DP) packages

Table 1. Device selection summary

Feature	PCA9507	PCA9508	PCA9509	PCA9512A	PCA9517A	PCA9519	PCA9527
$V_{CC(A)}$ range	2.7 V to 5.5 V	0.9 V to 5.5 V	1.1 V to $V_{CC(B)}$ − 1 V	2.7 V to 5.5 V	0.9 V to 5.5 V	1.1 V to $V_{CC(B)}$ − 1 V	2.7 V to 5.5 V
$V_{CC(B)}$ range	2.7 V to 5.5 V	2.7 V to 5.5 V	3.0 V to 5.5 V	2.7 V to 5.5 V	2.7 V to 5.5 V	3.0 V to 5.5 V	2.7 V to 5.5 V
Rise time accelerator on SDA and SCL lines	yes	-	-	yes	-	yes	-
Normal I/O	A side	A side	A side	[1]	A side	A side	A side
Static level offset	B side	B side	B side	[1]	B side	B side	B side

[1] Incremental offset (hybrid) type on both sides.

1.4 Pin functions

1.4.1 PCA9507/08/09/12A/17A/27

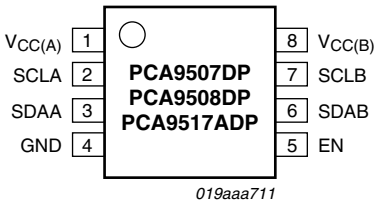


Fig 2. Device pinout for PCA9507/08/17A

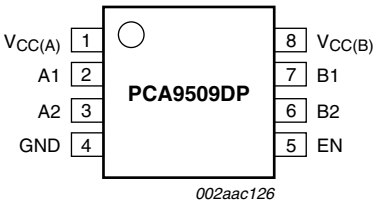


Fig 3. Device pinout for PCA9509

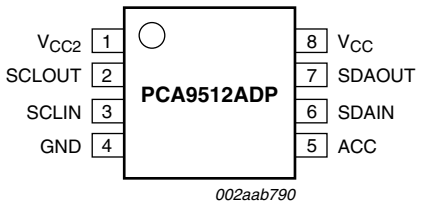


Fig 4. Device pinout for PCA9512A

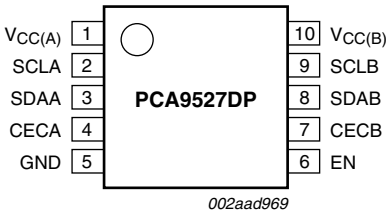


Fig 5. Device pinout for PCA9527

Table 2. Pin description for PCA9507/08/17A

Symbol	Pin	Description
$V_{CC(A)}$	1	port A supply voltage (0.9 V to 5.5 V)
SCLA	2	serial clock port A bus
SDAA	3	serial data port A bus
GND	4	supply ground (0 V)
EN	5	active HIGH repeater enable input
SDAB	6	serial data port B bus
SCLB	7	serial clock port B bus
$V_{CC(B)}$	8	port B supply voltage (2.7 V to 5.5 V)

Table 3. Pin description for PCA9509

Symbol	Pin	Description
$V_{CC(A)}$	1	port A power supply
A1[1]	2	port A (lower voltage side)
A2[1]	3	port A (lower voltage side)
GND	4	ground (0 V)
EN	5	enable input (active HIGH)
B2[1]	6	port B (SMBus/I²C-bus side)
B1[1]	7	port B (SMBus/I²C-bus side)
$V_{CC(B)}$	8	port B power supply

[1] Port A and port B can be used for either SCL or SDA.

Table 4. Pin description for PCA9512A

Symbol	Pin	Description
V_{CC2}	1	Supply voltage for devices on the card I²C-bus. Connect pull-up resistors from SDAOUT and SCLOUT to this pin.
SCLOUT	2	serial clock output to and from the SCL bus on the card
SCLIN	3	serial clock input to and from the SCL bus on the backplane
GND	4	ground supply; connect this pin to a ground plane for best results.
ACC	5	CMOS threshold digital input pin that enables and disables the rise time accelerators on all four SDAn and SCLn pins. ACC enables all accelerators when set to V_{CC2}, and turns them off when set to GND.
SDAIN	6	serial data input to and from the SDA bus on the backplane
SDAOUT	7	serial data output to and from the SDA bus on the card
V_{CC}	8	supply voltage; from the backplane, connect pull-up resistors from SDAIN and SCLIN to this pin.

Table 5. Pin description for PCA9527

Symbol	Pin	Description
$V_{CC(A)}$	1	port A supply voltage (2.7 V to 5.5 V)
SCLA	2	serial clock port A bus with rise time accelerator for DDC line or cable, 5 V tolerant
SDAA	3	serial data port A bus with rise time accelerator for DDC line or cable, 5 V tolerant
CECA	4	serial data with normal I/O powered by $V_{CC(B)}$, 5 V tolerant
GND	5	supply ground (0 V)
EN	6	active HIGH buffer enable input
CECB	7	serial data with static level offset, powered by $V_{CC(B)}$, 5 V tolerant
SDAB	8	serial data port B bus with static level offset, 5 V tolerant
SCLB	9	serial clock port B bus with static level offset, 5 V tolerant
$V_{CC(B)}$	10	port B supply voltage (2.7 V to 3.6 V)

1.4.2 PCA9519

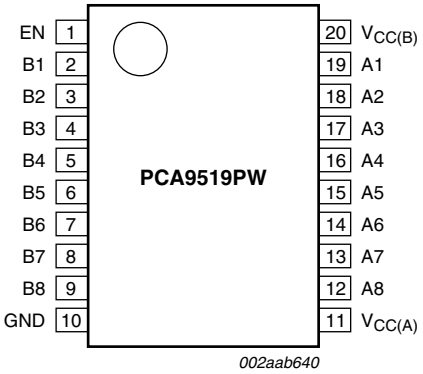


Fig 6. Device pinout for PCA9519

Table 6. Pin description for PCA9519

Symbol	Pin	Description
EN	1	enable input (active HIGH)
B1	2	B1 port (SMBus/I²C-bus side)[1]
B2	3	B2 port (SMBus/I²C-bus side)[1]
B3	4	B3 port (SMBus/I²C-bus side)[1]
B4	5	B4 port (SMBus/I²C-bus side)[1]
B5	6	B5 port (SMBus/I²C-bus side)[1]
B6	7	B6 port (SMBus/I²C-bus side)[1]
B7	8	B7 port (SMBus/I²C-bus side)[1]
B8	9	B8 port (SMBus/I²C-bus side)[1]
GND	10	ground (0 V)
$V_{CC(A)}$	11	port A power supply
A8	12	A8 port (low voltage side)[1]
A7	13	A7 port (low voltage side)[1]
A6	14	A6 port (low voltage side)[1]
A5	15	A5 port (low voltage side)[1]
A4	16	A4 port (low voltage side)[1]
A3	17	A3 port (low voltage side)[1]
A2	18	A2 port (low voltage side)[1]
A1	19	A1 port (low voltage side)[1]
$V_{CC(B)}$	20	port B power supply

[1] Port A and port B can be used for either SCL or SDA.

1.5 Ordering information

Table 7. Ordering information

Package	Container	PCA9507	PCA9508	PCA9509	PCA9512A	PCA9517A	PCA9519	PCA9527
SO8	tube[1]	PCA9507D	PCA9508D	PCA9509D	PCA9512AD	PCA9517AD	-	-
	tape and reel[2]	PCA9507D	PCA9508D	PCA9509D	PCA9512AD	PCA9517AD	-	-
TSSOP8	tape and reel[2]	PCA9507DP	PCA9508DP	PCA9509DP	PCA9512ADP	PCA9517ADP	-	-
XQFN8U	reel pack, reverse[3]	-	-	PCA9509GM	-	-	-	-
TSSOP10	tape and reel[2]	-	-	-	-	-	-	PCA9527DP
TSSOP20	tape and reel[2]	-	-	-	-	-	PCA9519PW	-
HVQFN24	tape and reel[2]	-	-	-	-	-	PCA9519BS	-

[1] For “tube” container orders, append “,112” to type number.

[2] For “tape and reel” container orders, append “,118” to type number.

[3] For “reel pack, reverse” orders, append “,125” to type number.

Additional information on packages including outline dimensions, Moisture Sensitivity Level (MSL) ratings, $R_{th(j-a)}$ can be obtained at www.nxp.com/thermaldata/.

1.6 Data sheets and IBIS/SPICE models

Data sheets and IBIS models can be downloaded from www.nxp.com/edafiles/.

SPICE models require a device-specific Non-Disclosure Agreement (NDA), which can be requested at www.nxp.com/spice_circuit_models/.

2. Technical information

2.1 Block diagrams and features

2.1.1 PCA9507 features

- Two channel, bidirectional buffer isolates capacitance allowing 1400 pF on port A and 400 pF on port B
- Exceeds 18 meters (above the maximum distance for HDMI DDC)
- Rise time accelerator and normal I/O on port A
- Static level offset on port B
- Voltage level translation from 2.7 V to 5.5 V

The block diagram for the PCA9507 is shown in Figure 7.

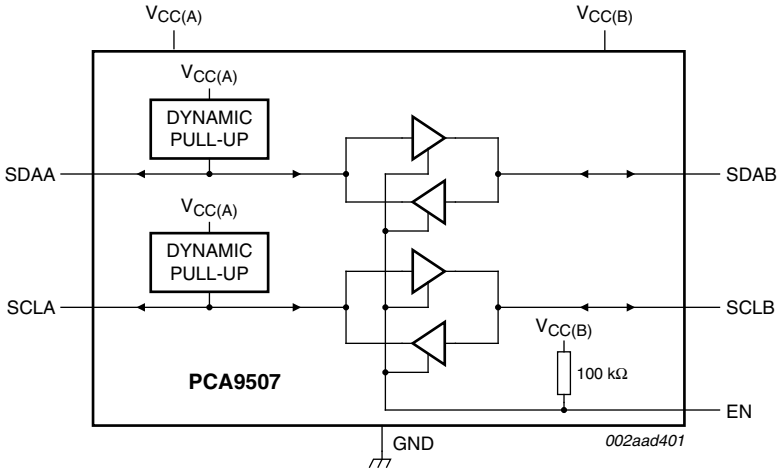


Fig 7. PCA9507 block diagram

2.1.2 PCA9508 features

- Two channel, bidirectional buffer isolates capacitance and allows 400 pF on either side of the device
- Supports offset-free hot-swap with IDLE/STOP detect circuitry
- Voltage level translation from 0.9 V to 5.5 V and from 2.7 V to 5.5 V
- Static level offset on B side
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Powered-off high-impedance I²C-bus pins

The block diagram for the PCA9508 is shown in Figure 8.

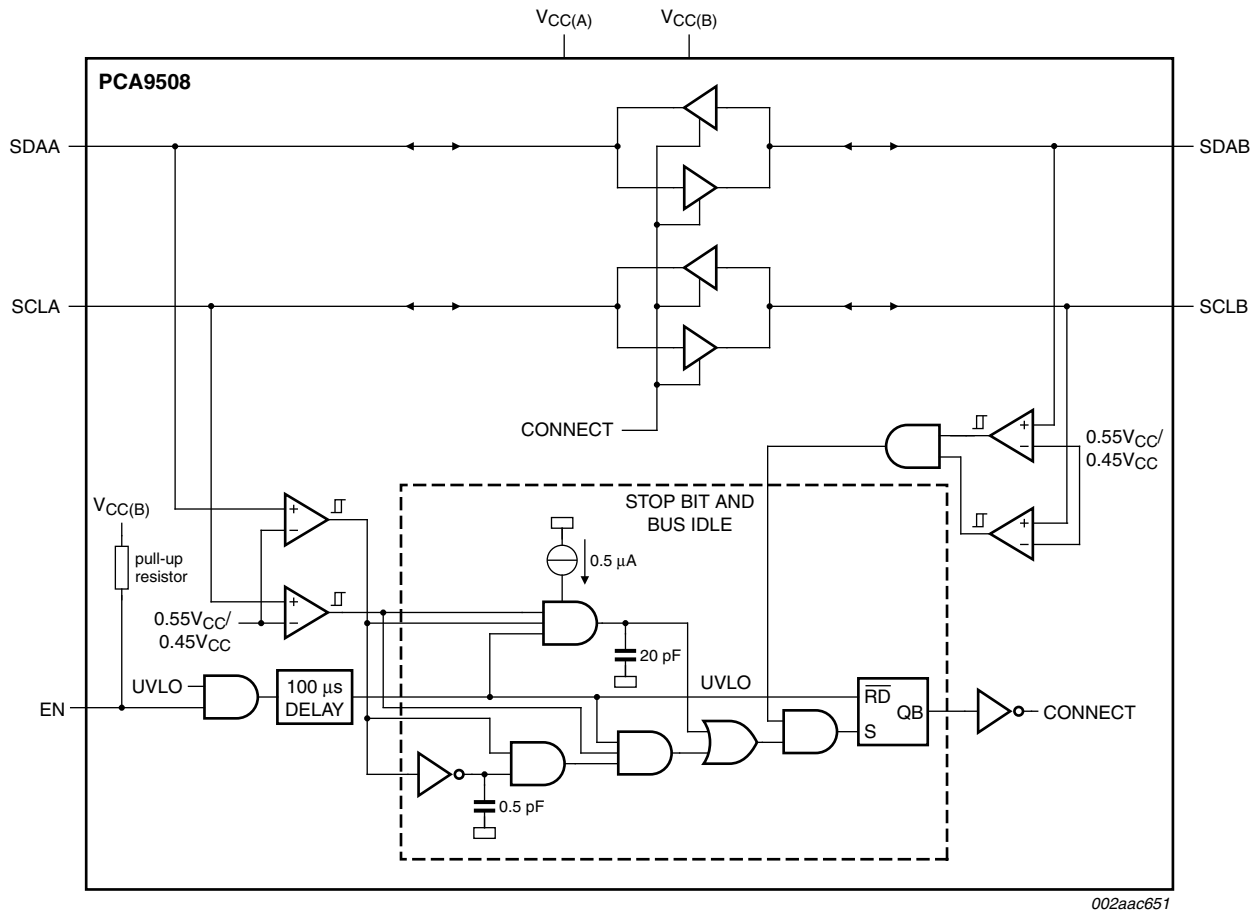


Fig 8. PCA9508 block diagram

2.1.3 PCA9509 features

- Bidirectional buffer isolates capacitance and allows 400 pF on port B of the device
- Voltage level translation from port A (1 V [0.95 V in special cases] to $V_{CC(B)}$ − 1.0 V) to port B (3.0 V to 5.5 V)
- Requires no external pull-up resistors on lower voltage port A
- Supports arbitration and clock stretching across the repeater

The block diagram for the PCA9509 is shown in Figure 9.

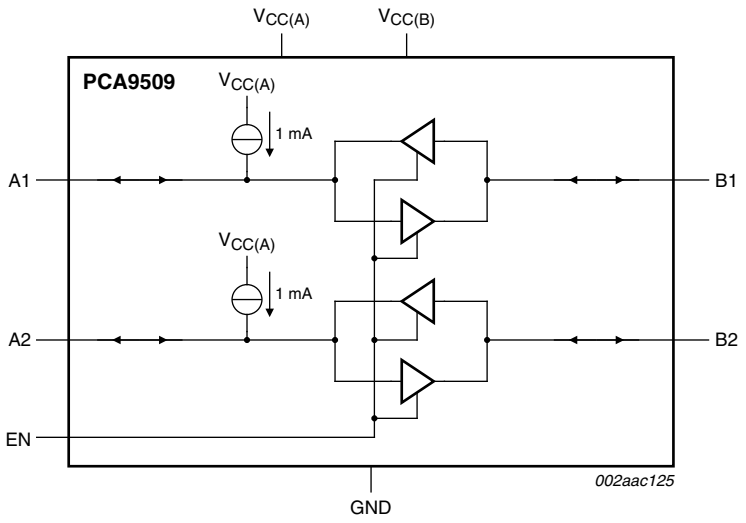


Fig 9. PCA9509 block diagram

2.1.4 PCA9512A features

- Bidirectional buffer for SDA and SCL lines increases fan-out and prevents SDA and SCL corruption during live board insertion and removal from multipoint backplane systems
- Compatible with I²C-bus Standard-mode, I²C-bus Fast-mode, and SMBus standards
- Built-in ΔV/Δt rise time accelerators on all SDA and SCL lines (0.6 V threshold) with ability to disable ΔV/Δt rise time accelerator through the ACC pin for lightly loaded systems, requires the bus pull-up voltage and respective supply voltage (V_{CC} or V_{CC2}) to be the same
- 5 V to 3.3 V level translation with optimum noise margin
- High-impedance SDAn and SCLn pins for V_{CC} or V_{CC2} = 0 V
- 1 V precharge on all SDAn and SCLn pins
- Supports clock stretching and multiple master arbitration and synchronization
- Operating power supply voltage range: 2.7 V to 5.5 V
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

- Packages offered: SO8, TSSOP8 (MSOP8)

The block diagram for PCA9512A is shown in Figure 10.

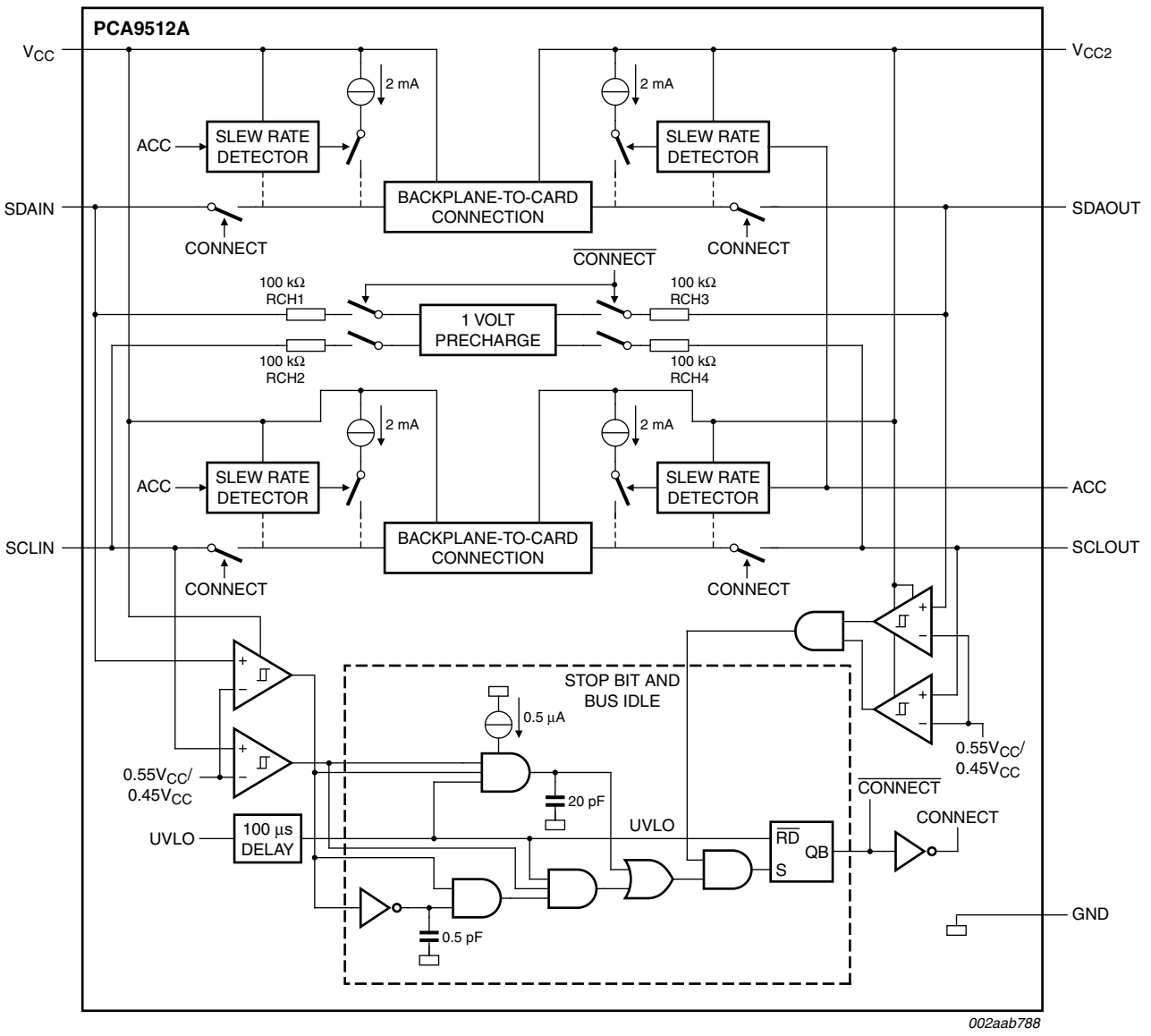


Fig 10. PCA9512A block diagram

2.1.5 PCA9517A features

- Two channel, bidirectional buffer isolates capacitance and allows 400 pF on either side of the device
- Active HIGH enable input
- Voltage level translation from 0.9 V to 5.5 V and from 2.7 V to 5.5 V
- Supports arbitration and clock stretching

The block diagram for the PCA9517A is shown in Figure 11.

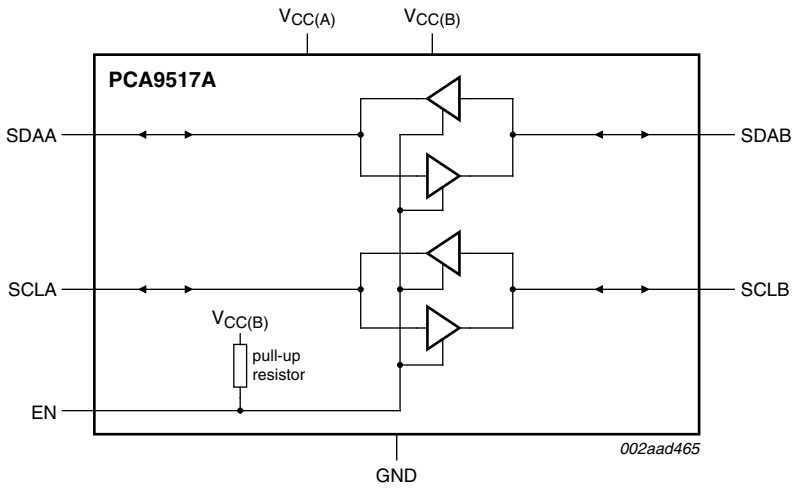


Fig 11. PCA9517A block diagram

2.1.6 PCA9519 features

- Four channel (4 SCL/SDA pairs), bidirectional buffer isolates capacitance and allows 400 pF on port B of the device
- Voltage level translation from port A (1 V to $V_{CC(B)}$ − 1.5 V) to port B (3.0 V to 5.5 V)
- Requires no external pull-up resistors on lower voltage port A
- Active HIGH enable input
- Supports arbitration and clock stretching
- 50 ns glitch filter on B-side input

The block diagram for the PCA9519 is shown in Figure 12.

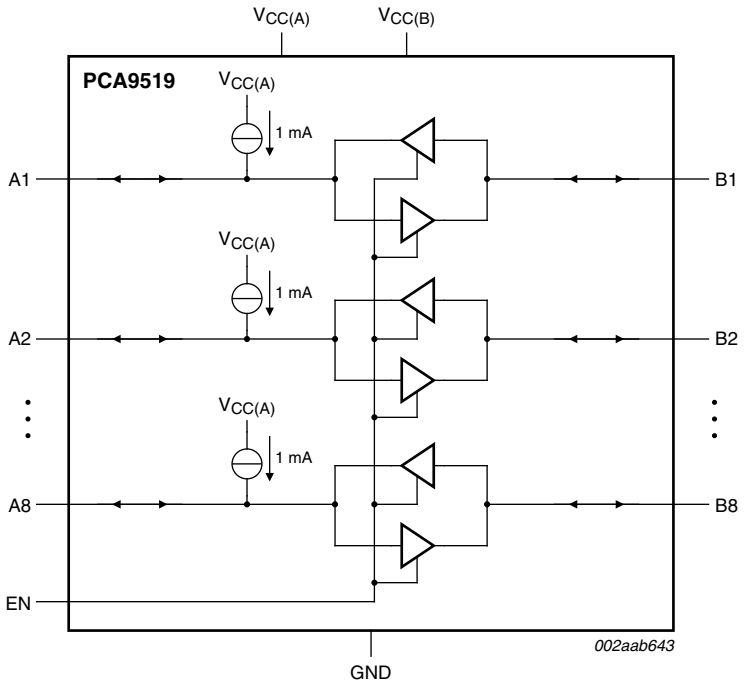


Fig 12. PCA9519 block diagram

2.1.7 PCA9527 features

- Three channel, bidirectional buffer isolates capacitance allowing 1400 pF on port A and 400 pF on port B
- Exceeds 18 meters (above the maximum distance for HDMI DDC)
- Rise time accelerator and normal I/O on port A (no accelerator for CEC)
- Static level offset on port B
- Voltage level translation from 2.7 V to 5.5 V
- CEC is 5 V tolerant, powered by $V_{CC(B)}$
- Active HIGH buffer enable input
- Supports arbitration and clock stretching

The block diagram for the PCA9527 is shown in Figure 13.

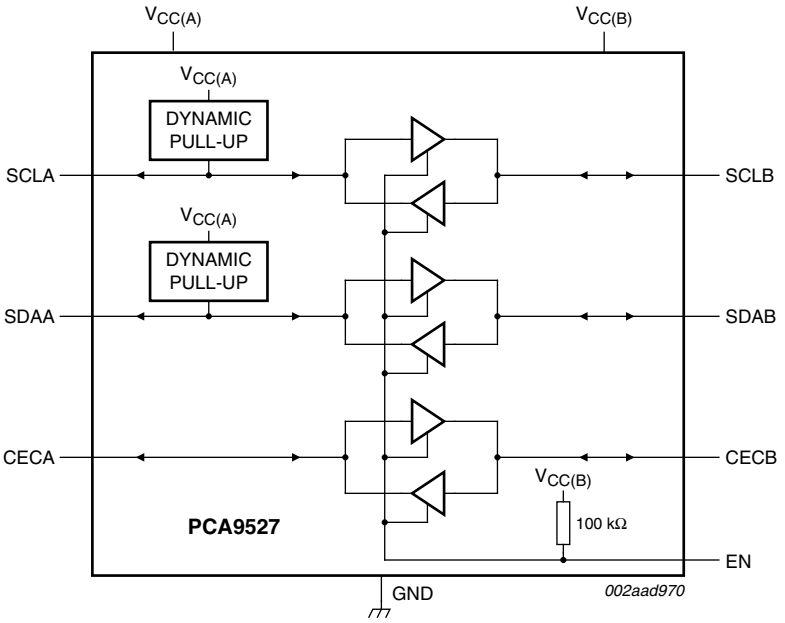


Fig 13. PCA9527 block diagram

2.2 Operation

2.2.1 Start-up (PCA9512A)

When the PCA9512A device first receives power on its V_{CC} pin, either during power-up or during level shifting, it starts in an UnderVoltage LockOut (UVLO) state, ignoring any activity on the SDA and SCL pins until V_{CC} rises above 2.5 V. PCA9512 also waits for V_{CC2} to rise above 2 V. This ensures that the part does not try to function until it has enough voltage to do so. During this time, the 1 V precharge circuitry is active and forces 1 V through internal 100 kΩ nominal resistors to the SDA and SCL pins.

Once the PCA9512A comes out of the UVLO state, it is assumed that SDAIN and SCLIN have been hot swapped into a live system and that SDAOUT and SCLOUT are being powered up at the same time as the devices themselves. Therefore, they look for either a STOP command or a bus idle condition on the backplane side to indicate the completion of a data transaction. When either one occurs, the parts also verify that both the SDAOUT and SCLOUT voltages are HIGH. When all of these conditions are met, the input-to-output connection circuitry is activated, joining the SDA and SCL buses on the I/O card with those on the backplane.

PCA9507/09/17A/19/27 do not have idle bus detect circuitry.

2.2.2 Connection circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A LOW forced on either pin at any time results in both pin voltages being LOW. SDAIN and SDAOUT enter a logic HIGH state only when all devices on both SDAIN and SDAOUT force a HIGH. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the PCA9507/08/09/12A/17A/19/27.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the opposing port capacitances isolated. Because of this isolation, the waveforms on the buses look slightly different.

2.2.3 Input to output offset voltage

PCA9507/08/09/17A/19/27's are static offset buffers and PCA9512A is an incremental offset (hybrid) buffer.

2.2.4 Propagation delays

PCA9507 has rise time accelerators on port A only. During port A positive bus transitions a current source is switched on to quickly slew the SDAA and SCLA lines HIGH once the input level of $0.3V_{CC(A)}$ is exceeded for the PCA9507 and turns off as the $0.7V_{CC(A)}$ voltage is approached.

PCA9527 has rise time accelerators on port A of SCL and SDA only; the CECA pin does not have a rise time accelerator. During port A positive bus transitions a current source is switched on to quickly slew the SDAA and SCLA lines HIGH once the input level of $0.3V_{CC(A)}$ is exceeded for the PCA9527 and turns off as the $0.7V_{CC(A)}$ voltage is approached.

During a rising edge, the rise time on each side is determined by the combined pull-up current of the PCA9507/27 boost current, the bus resistor and the equivalent capacitance on the line. If the pull-up currents are the same, a difference in rise time occurs which is directly proportional to the difference in capacitance between the two sides.

2.2.5 Rise time accelerators (PCA9507/PCA9527)

Once connection between the two sides has been established, rise time accelerator circuits on port A side SDA and SCL pins are activated. These allow the user to choose weaker DC pull-up currents on the bus, reducing power consumption while still meeting system rise time requirements. During positive bus transitions, the PCA9507/27 devices switch a 2 mA current source to quickly slew the SDA and SCL lines once their DC voltages exceed 0.6 V.

Using a general rule of 20 pF of capacitance for every device on the bus (10 pF for the device and 10 pF for interconnect), choose a pull-up current so that the bus will rise on its own at a rate of at least 1.25 V/μs to guarantee activation of the rise time accelerators.

For example, assume an SMBus system with V_{CC} = 3.3 V, a 10 kΩ pull-up resistor and an equivalent bus capacitance of 200 pF. The rise time of an SMBus system is calculated from ($V_{IL(max)}$ − 0.15 V) to ($V_{IH(min)}$ + 0.15 V), or 0.65 V to 2.25 V. It takes 0.92 × RC time constant to traverse this voltage for a 3.3 V supply; in this case,
0.92 × (10 kΩ × 200 pF) = 1.85 ms. Thus, the system exceeds the maximum allowed rise time of 1 ms by 85 %. However, using the rise time accelerators, which are activated at a DC threshold of below 0.65 V, the worst-case rise time is:
(2.25 V − 0.65 V) × 200 pF / 1 mA = 320 ns, which meets the 1 μs rise time requirement.

2.2.6 Enable low current disable (PCA9507/08/09/17A/19/27 only)

The enable pin (EN) is active HIGH with an internal pull-up to $V_{CC(B)}$ and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I²C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C-bus parts being enabled. The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

For PCA9508/12A only, if enabled while the bus is active, the PCA9508/12A will connect at the first STOP signal or at the first gap in activity that satisfies the internal idle bus time.

2.3 Design constraints

2.3.1 Maximum current

The bus IR drops must be controlled such that the device sees 0.4 V or less V_{IL} during a contention condition or clock-stretching event.

2.3.2 5 V bus operation

The bus pull-up resistors need to be tied to the 5 V supply if any 5 V parts are on the bus to guarantee that the V_{IH} of the 5 V device is reached. If no 5 V parts are used, a 3.3 V bus pull-up resistor supply should be used as this will result in a smaller RC time constant for the same 3 mA current.

2.3.3 Operation at 400 kHz

Fast-mode parts can only be operated at 400 kHz clock frequency if no Standard-mode parts are on the bus. The maximum acceptable capacitive load for 400 kHz operation with a 3 mA current is 331 pF at V_{pu} = 3.3 V ± 0.3 V, and 208 pF at V_{pu} = 5.0 V ± 0.5 V, in order to satisfy the Fast-mode rise time requirement. (V_{pu} is pull-up voltage.)

2.3.4 Rise time

Rise time must be less than or equal to 1000 ns because the device regenerates the I²C-bus signal, the pull-up voltages on either side need not be equal, that is, one side could be 5 V ± 0.5 V and the other side could be 3.3 V ± 0.3 V.

2.3.5 Device segment enable

Only enable or disable the devices when all buses are in an idle state, to prevent system failures.

2.3.6 Resistor pull-up value selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/μs on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value $R_{PU(max)}$ using Equation 1:

$$R_{PU(max)} < 800 \times 10^3 \frac{V_{CC(min)} - 0.6}{C_b} \quad (1)$$

Where:

$R_{PU(max)}$ = the pull-up resistor value in Ω

$V_{CC(min)}$ = the minimum V_{CC} voltage

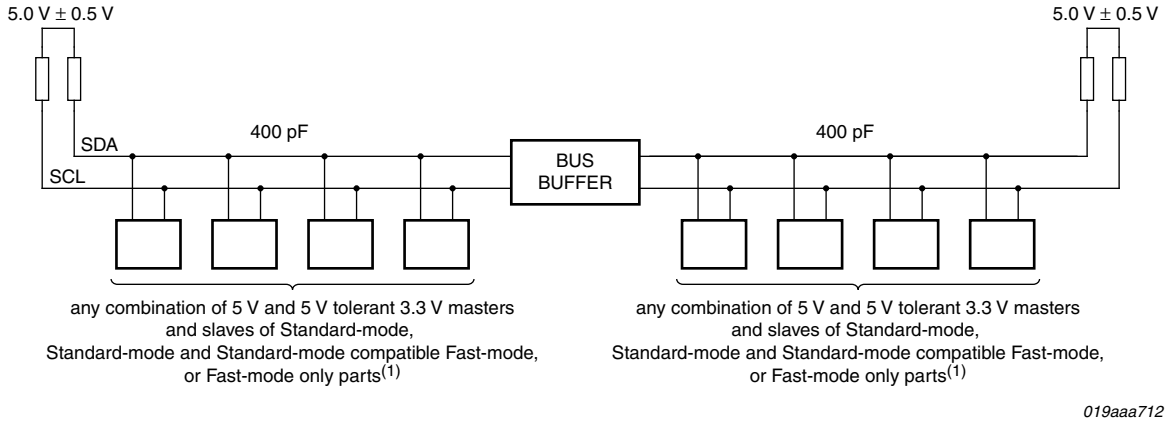
C_b = the equivalent bus capacitance in pF

3. Applications

3.1 Bus expansion beyond the 400 pF limitation

Adding more I²C-bus and SMBus devices on the bus may exceed the 400 pF limitation. The PCA9507/08/09/12A/17A/19/27 can isolate device and trace capacitance to different segments that are 400 pF or less capacitive loading so that the I²C-bus and SMBus devices can operate properly. A typical PCA9507/08/09/12A/17A/19/27 application is shown in Figure 14.

If all masters are on one side of the PCA9507/08/09/12A/17A/19/27 bus buffer and none of the slaves on the other side of the bus buffer use clock stretching and if all of these slaves are capable of 6 mA I_{OL}, then the slave side pull-up can be sized for 6 mA because there will be no contention nor clock stretching to be communicated by the bus buffer.



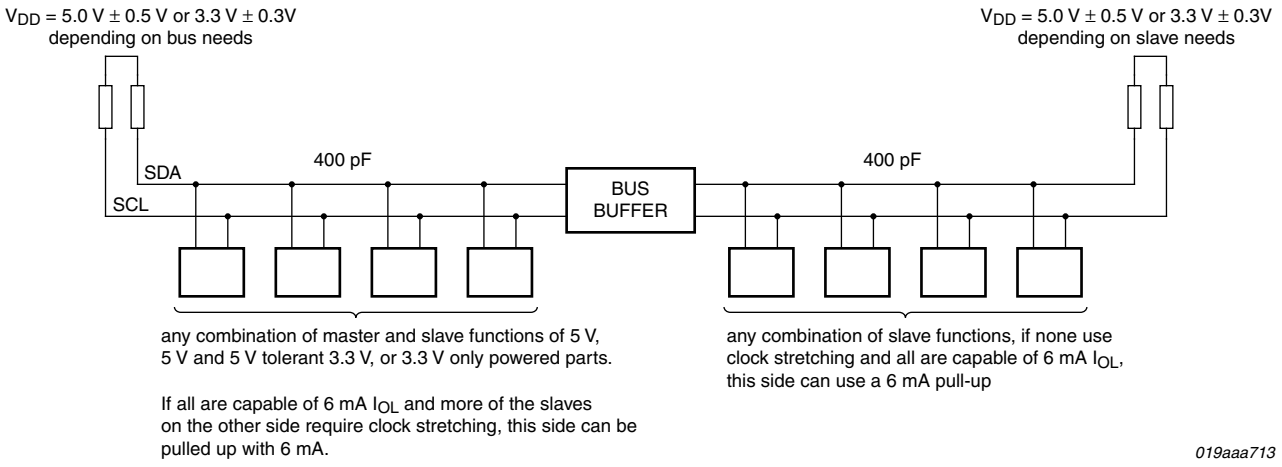
(1) All parts must be Fast-mode to run at 400 kHz.

Fig 14. Typical bus expansion application

3.2 Split bus 100 kHz and 400 kHz application

If all of the masters and slaves on the master side of the PCA9507/08/09/12A/17A/19/27 are capable of Fast-mode operation, none of the slaves on the opposite side of the bus buffer require clock stretching and the master(s) is(are) able to generate enable and disable changes during the bus idle time, then the enable feature of the PCA9507/08/09/12A/17A/19/27 could be used to isolate the master side to allow the master to run at 400 kHz rather than the Standard-mode 100 kHz necessary when any Standard-mode slave are present on the slave side of the repeater.

If an individual slave is particularly badly behaved during power-up but performs correctly after power-up, or power-up and system reset on power-up, then the PCA9507/08/09/12A/17A/19/27 enable function could be used to isolate the offending part until it is well behaved and both sides of the bus buffer are in an idle state. The enable should never be changed, enabled nor disabled, except when both sides of the bus buffer are in an idle state. If the part being isolated is a slave that does not use clock stretching, then the isolation technique and the standard bus expansion technique can be combined.



(1) All parts must be Fast-mode to run at 400 kHz.

Fig 15. PCA9507/08/09/12A/17A/19/27 in split bus 100 kHz and 400 kHz application

3.3 Voltage level shifting

A typical application PCA9507 is shown in Figure 16. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 5 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus. When port A of the PCA9507 is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.3V_{CC(A)}$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5 V. When port B of the PCA9507 falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground.

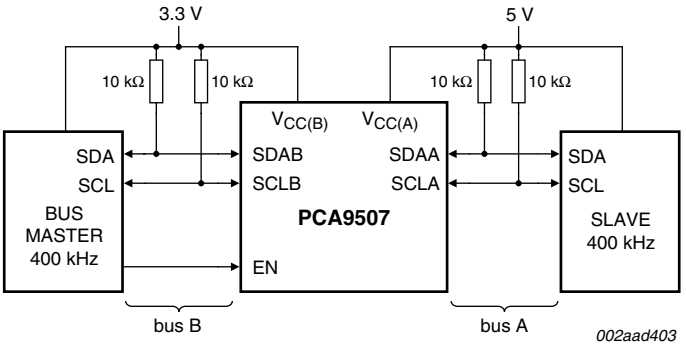


Fig 16. Typical application for PCA9507

A typical application for PCA9508 is shown in Figure 17. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 1.2 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus. When the A side of the PCA9508 is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.5V_{CC(A)}$ and causes the internal driver on the B side to turn on, causing the B side to pull down to about 0.5 V. When the B side of the PCA9508 falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A side pin down to ground.

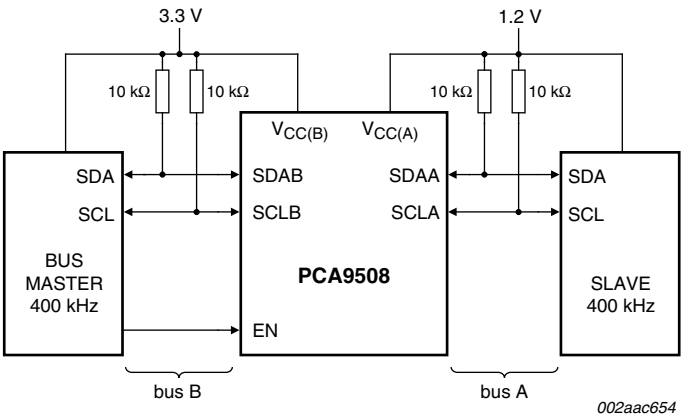


Fig 17. Typical application for PCA9508

A typical application for PCA9509 is shown in Figure 18. In this example, the CPU is running on a 1.1 V I²C-bus while the master is connected to a 3.3 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus. When port B of the PCA9509 is pulled LOW by a driver on the I²C-bus, a CMOS hysteresis detects the falling edge when it goes below $0.3V_{CC(B)}$ and causes the internal driver on port A to turn on, causing port A to pull down to about 0.2 V. When port A of the PCA9509 falls, first a comparator detects the falling edge and causes the internal driver on port B to turn on and pull the port B pin down to ground.

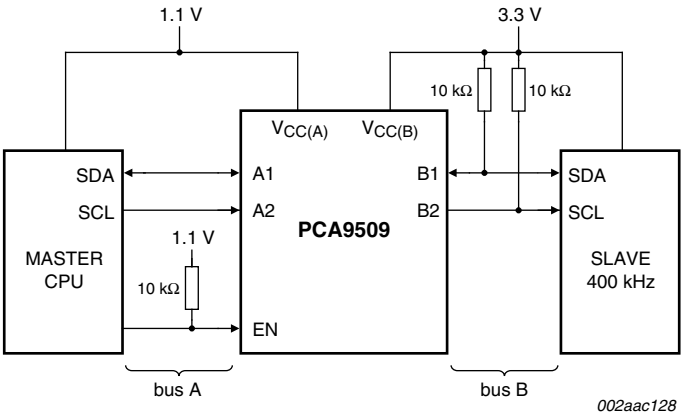


Fig 18. Typical application for PCA9509

A typical application for PCA9512A is shown in Figure 19. In this example, the system master is running on a 5 V I²C-bus while the slave is connected to a 3 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus. The PCA9512A is 5 V tolerant, so it does not require any additional circuitry to translate between 2.7 V to 5.5 V bus voltages. During positive bus transactions, a 2 mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.6 V for the PCA9512A is exceeded. The rising edge rate should be at least 1.25 V/μs to guarantee turn on of the accelerators. The built-in $\Delta V/\Delta t$ rise time accelerators on all SDA and SCL lines requires the bus pull-up voltage and respective supply voltage (V_{CC} or V_{CC2}) to be the same. The built-in $\Delta V/\Delta t$ rise time accelerators can be disabled through the ACC pin for lightly loaded systems.

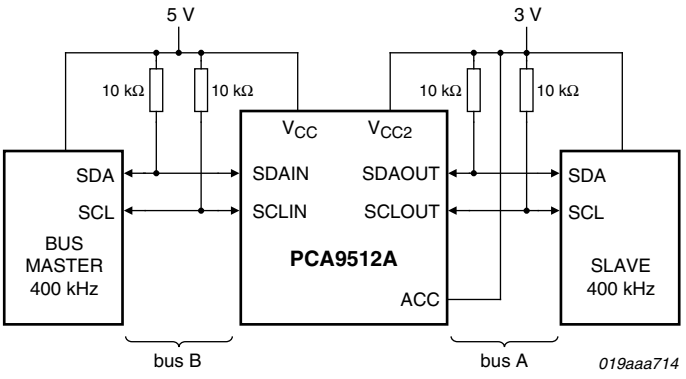


Fig 19. Typical application for PCA9512A

A typical application for PCA9517A is shown in Figure 20. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 1.2 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus. The PCA9517A is 5 V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.5 V bus voltages and 2.7 V to 5.5 V bus voltages. When the A-side of the PCA9517A is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.3V_{CCA}$ and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.5 V. When the B-side of the PCA9517A falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on the A-side to turn on and pull the A-side pin down to ground.

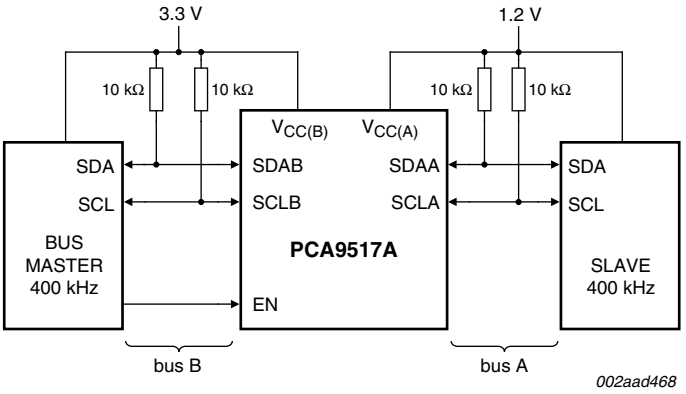


Fig 20. Typical application for PCA9517A

A typical application for PCA9519 is shown in Figure 21. In this example, the CPU is running on a 1.1 V I²C-bus while the master is connected to a 3.3 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus. When port B of the PCA9519 is pulled LOW by a driver on the I²C-bus, a CMOS hysteresis detects the falling edge when it goes below $0.3V_{CC(B)}$ and causes the internal driver on port A to turn on, causing port A to pull down to about 0.2 V. When port A of the PCA9519 falls, first a comparator detects the falling edge and causes the internal driver on port B to turn on and pull the port B pin down to ground.

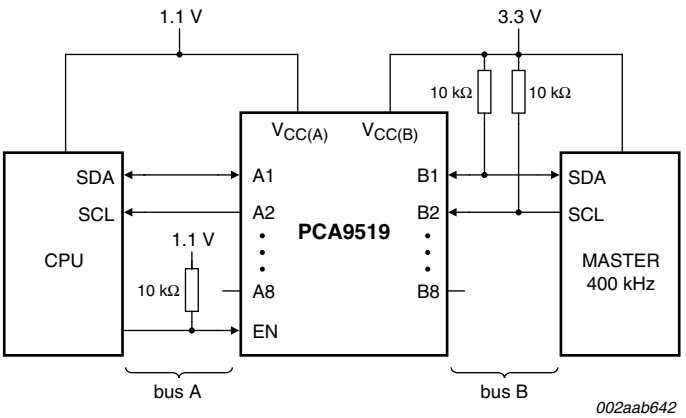


Fig 21. Typical application for PCA9519

A typical application for PCA9527 is shown in Figure 22. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 5 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus. When port A of the PCA9527 is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.3V_{CC(A)}$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5 V. When port B of the PCA9527 falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground.

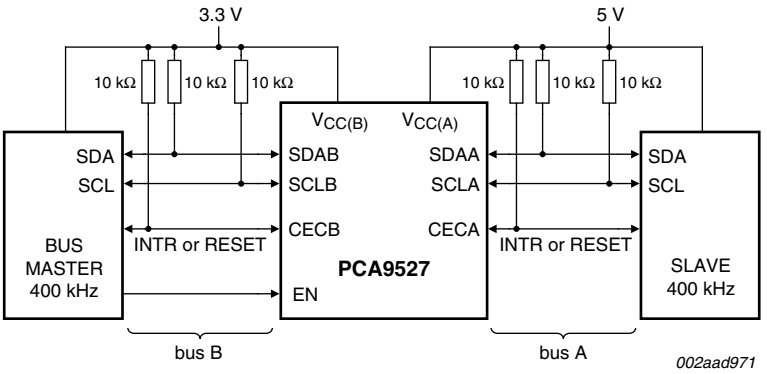


Fig 22. Typical application for PCA9527

HDMI DDC applications for DVD/R and LCD TV are shown in Figure 23 and Figure 24, respectively. In these applications the HDMI transmitter or receiver is 3.3 V, while the DDC line is 5 V, PCA9527 behaves like a voltage level shifter, a buffer and long cable bus extender to ensure signal integrity for accessing the EDID on the DDC line.

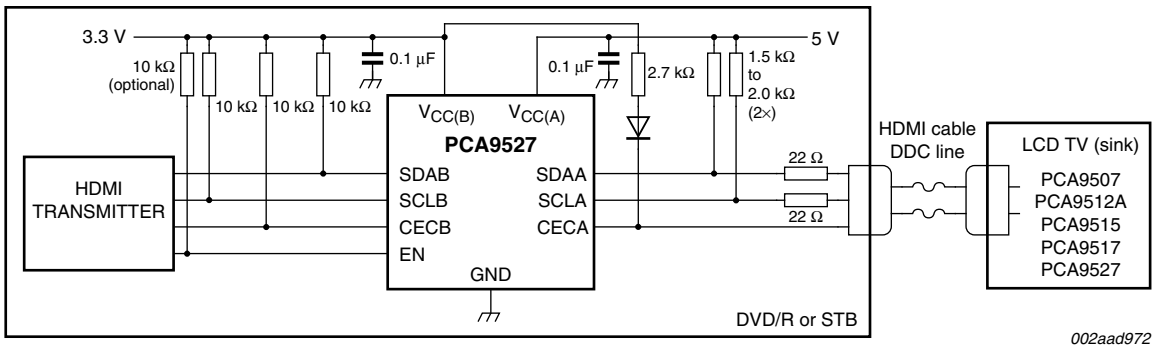


Fig 23. Source or DVD/R, STB application

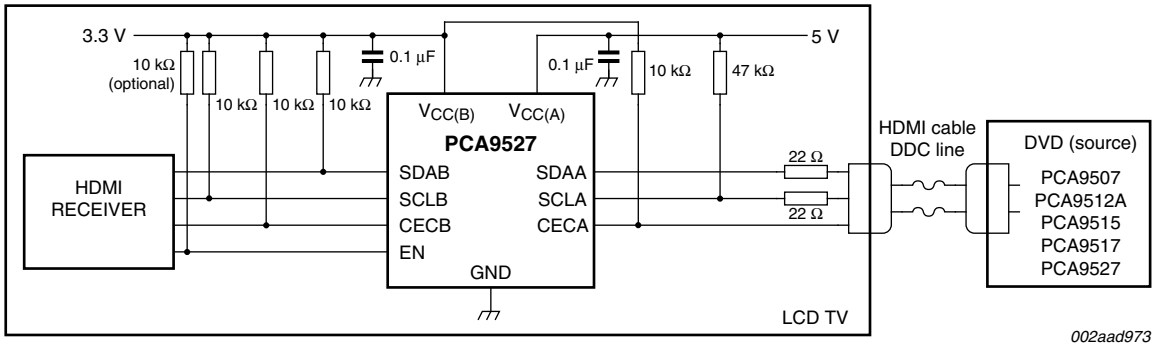


Fig 24. Sink or LCD TV application

The GTL2000/02/03/10, PCA9306 and NVT family of non-buffering devices allow I²C voltage level translation at any voltage between 1.0 V and 5.0 V to any voltage between 1.0 V and 5.0 V. See application note *AN10145, "Bidirectional low voltage translators"* for more information on the use of these passive devices to support voltage level translations. These GTL-TVC devices are less expensive than the PCA9507/08/09/12A/17A/19/27 level shifting bus buffers, but do not isolate the bus capacitance and rise time is dependant on the RC time constant.

Use of the I²C-bus in backplane systems is increasing and either a point-to-point arrangement with multiple individual buses to each line card from the master or a single multipoint bus to every line card is often used.

4. Additional information

The latest data sheets and IBIS models for the I²C-bus level shifting family of products and other I²C-bus and SMBus products can be found at the NXP Semiconductors web site www.nxp.com/ics/support/tools/.

Software tools for most of NXP Semiconductor I²C-bus products can be found at: www.nxp.com/redirect/demoboard.com.

Additional technical support for the I²C-bus and SMBus Repeater/Hub/Expander family of products and other I²C-bus and SMBus products can be requested by e-mailing the question to: **i2c.support@nxp.com**.

See *AN460, "Using the P82B96 for bus interface"* for further application information about P82B96.

See *AN255, "Introduction to I²C-bus enablers"* for further application information about all NXP I²C-bus buffers.

See *AN10145, "Bidirectional low voltage translators"* for further application information about GTL2000/02/10 bidirectional low voltage translators.

5. Abbreviations

Table 8. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
DDC	Data Display Channel
DVD/R	Digital Video Disc/Recorder
EDID	Extended Display Identification Data
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
HDMI	High Definition Media Interface
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LCD	Liquid Crystal Display
MM	Machine Model
MSL	Moisture Sensitivity Level
NDA	Non-Disclosure Agreement
PCI	Peripheral Component Interconnect
RC	Resistor-Capacitor network
SMBus	System Management Bus
TVC	Transceiver Voltage Clamps
UVLO	UnderVoltage LockOut

6. References

[1] **AN255, Introduction to I²C-bus enablers —** Application note; NXP Semiconductors

[2] **AN460, Using the P82B96 for bus interface —** Application note; NXP Semiconductors

[3] **AN10145, Bidirectional low voltage translators —** Application note; NXP Semiconductors

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8. Contents

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